

Gr 2826

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

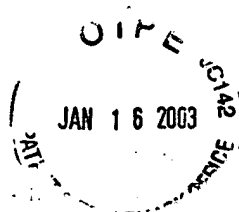
Applicant: Keith A. Joyner, et al.

Serial No: 10/068,014

Examiner: Victor A. Mandala

Filed: 02/05/2002

For: METHOD FOR MANUFACTURING AND STRUCTURE FOR TRANSISTORS WITH
REDUCED GATE TO CONTACT SPACING



Docket No: TI-29912

Conf. No: 7239

Art Unit: 2826

#4
Election
FONES
1-22-03

ELECTION

Assistant Commissioner for Patents
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 1-10-03.

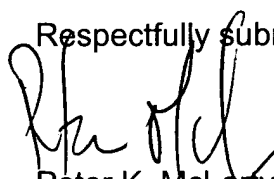

Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed December 16, 2002.

Applicants hereby elect to pursue Group II of Claims 1-14, drawn to method for manufacturing a transistor, without traversing the Examiner's restriction requirement.

Respectfully submitted,



Peter K. McLarty
Attorney for Applicants
Reg. No. 44,923

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